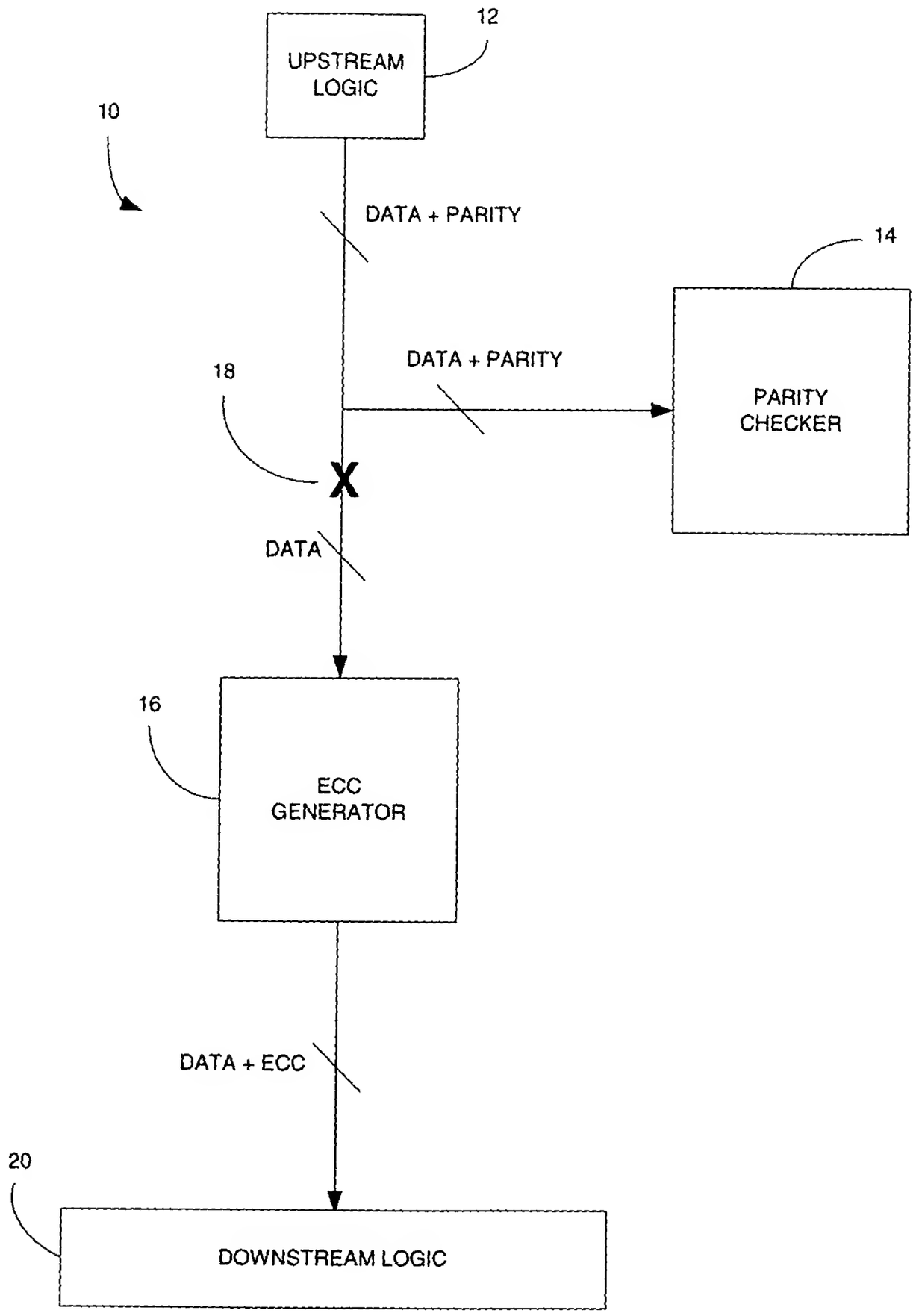

FIG. 1
PRIOR ART

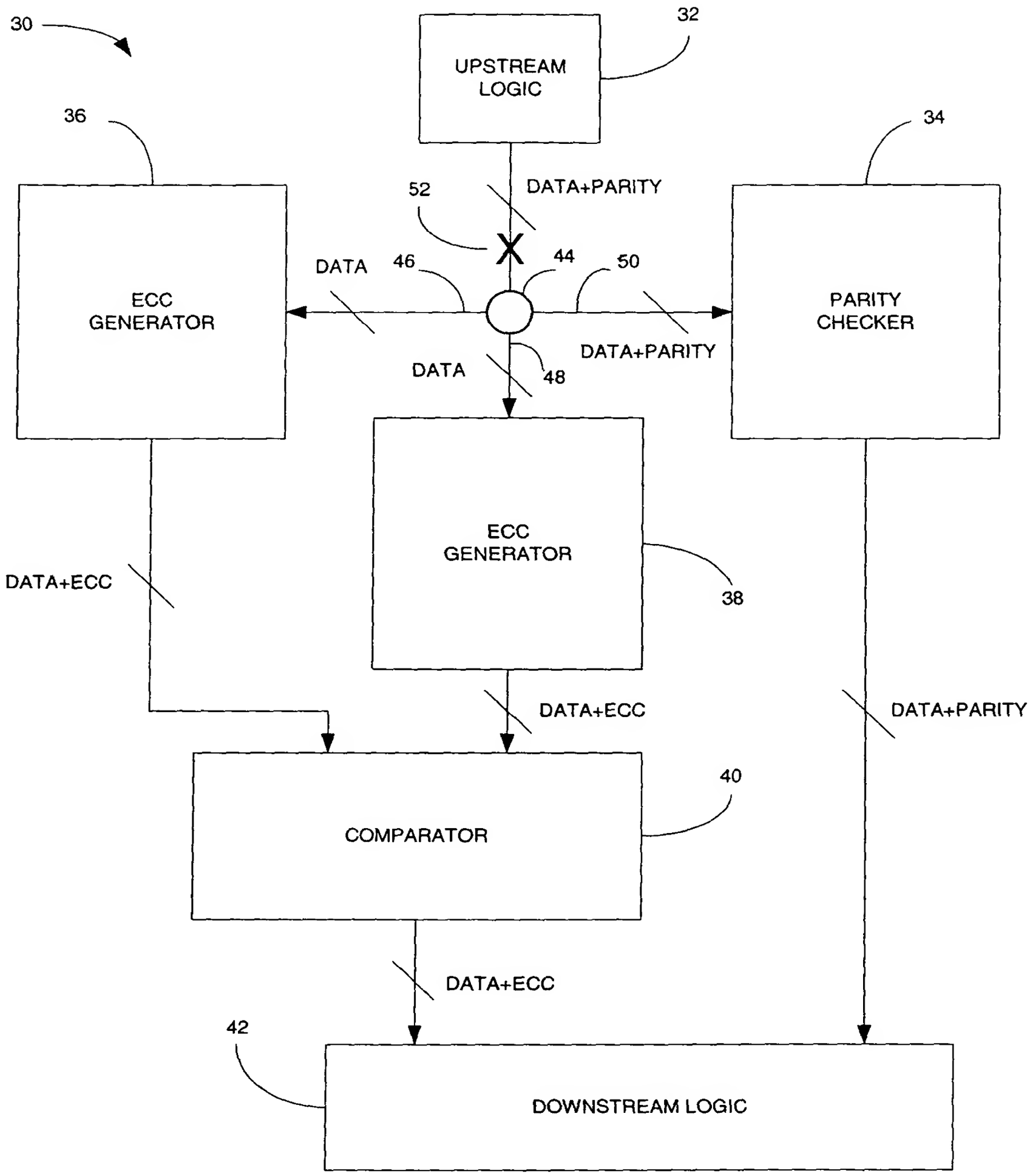

FIG. 2
PRIOR ART

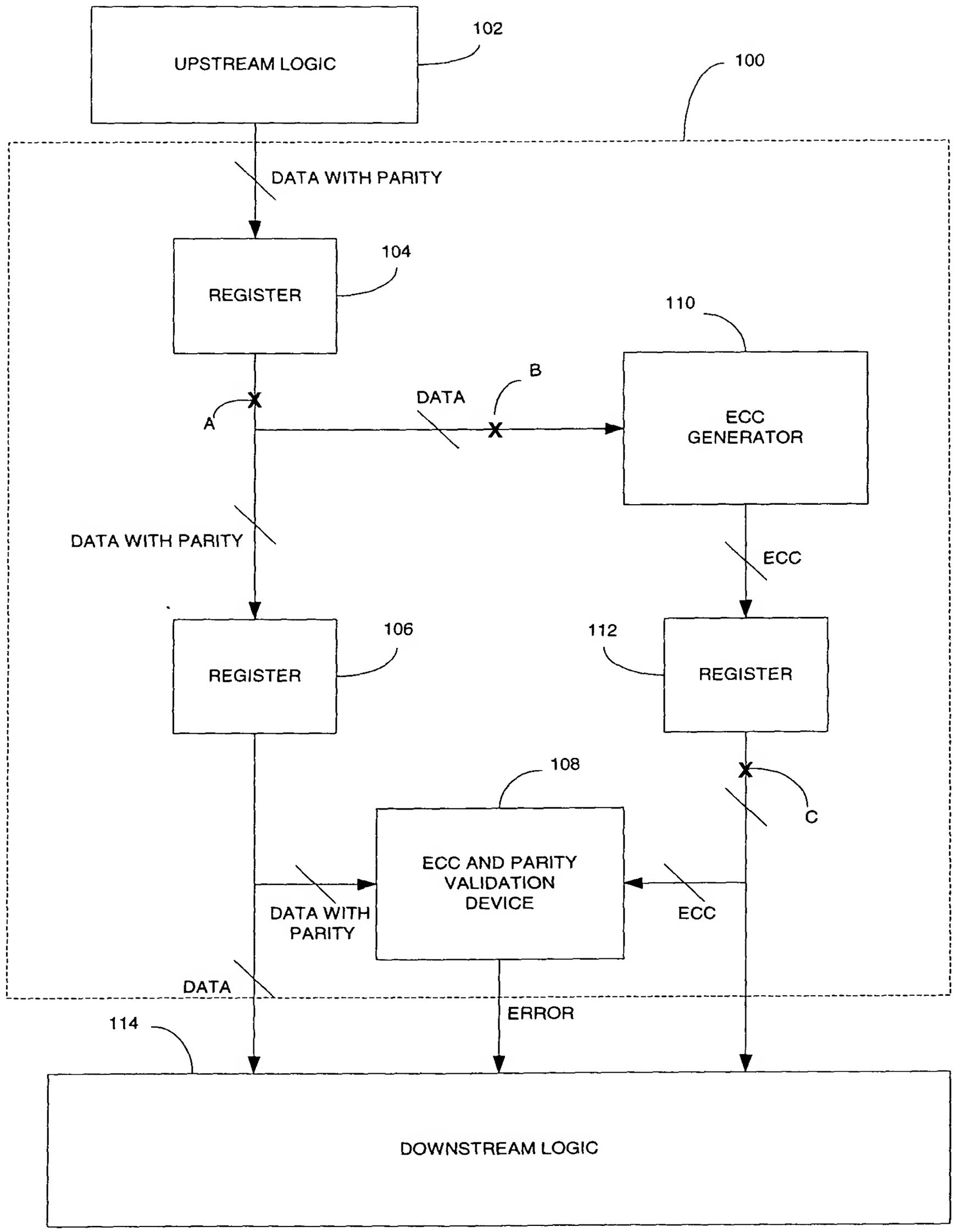
UPSTREAM LOGIC
102
100
DATA WITH PARITY
REGISTER
104
110
A
DATA
B
ECC
GENERATOR
DATA WITH PARITY
ECC
REGISTER
106
112
REGISTER
108
C
ECC AND PARITY
VALIDATION
DEVICE
DATA WITH
PARITY
ECC
DATA
ERROR
114
DOWNSTREAM LOGIC

FIG. 3

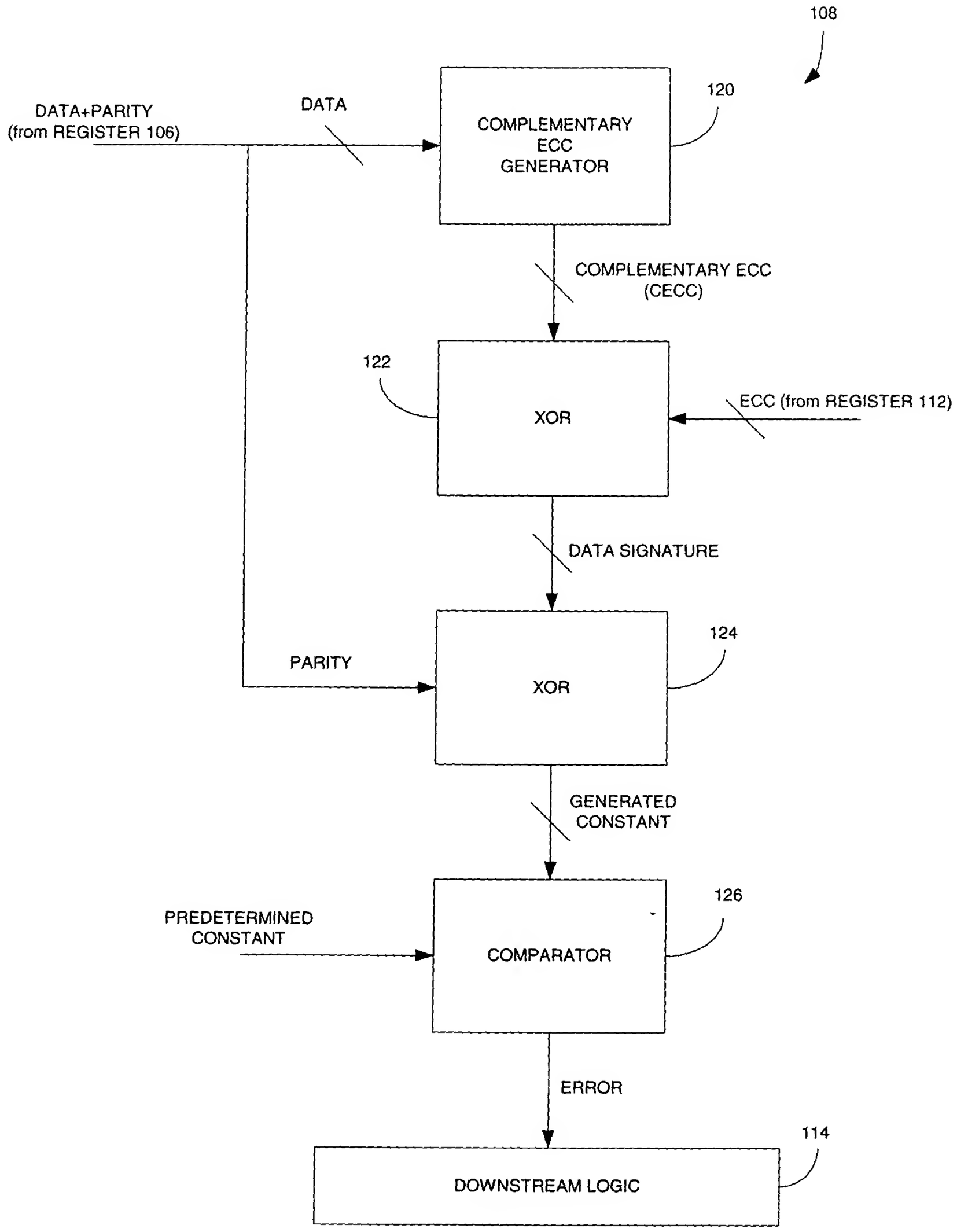
108
DATA+PARITY
(from REGISTER 106)
DATA
120
COMPLEMENTARY ECC GENERATOR
COMPLEMENTARY ECC (CECC)
122
XOR
ECC (from REGISTER 112)
DATA SIGNATURE
124
PARITY
XOR
GENERATED CONSTANT
126
PREDETERMINED CONSTANT
COMPARATOR
ERROR
114
DOWNSTREAM LOGIC

FIG. 4

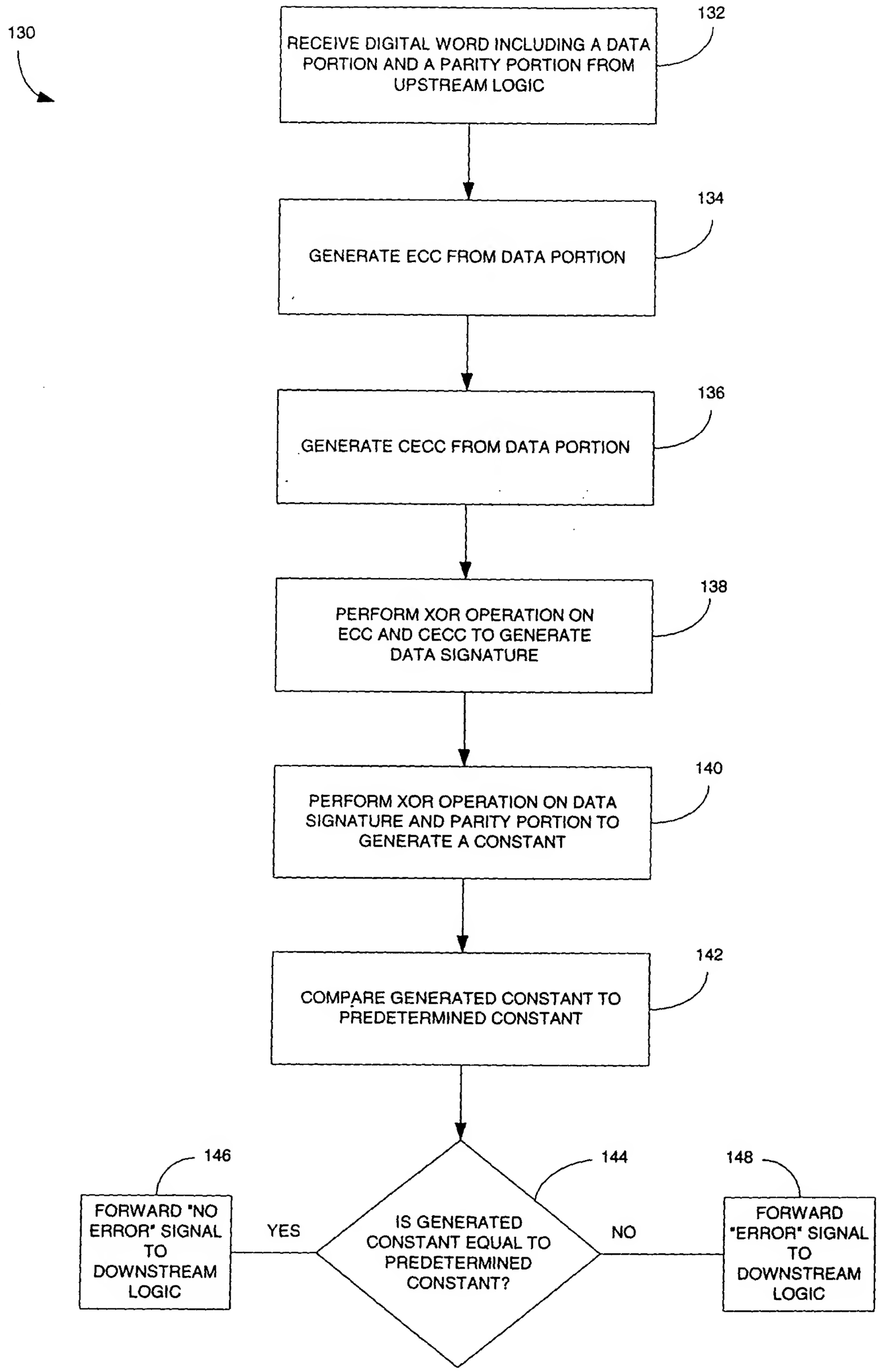
130
RECEIVE DIGITAL WORD INCLUDING A DATA PORTION AND A PARITY PORTION FROM UPSTREAM LOGIC
132
GENERATE ECC FROM DATA PORTION
134
GENERATE CECC FROM DATA PORTION
136
PERFORM XOR OPERATION ON ECC AND CECC TO GENERATE DATA SIGNATURE
138
PERFORM XOR OPERATION ON DATA SIGNATURE AND PARITY PORTION TO GENERATE A CONSTANT
140
COMPARE GENERATED CONSTANT TO PREDETERMINED CONSTANT
142
IS GENERATED CONSTANT EQUAL TO PREDETERMINED CONSTANT?
144
YES
NO
FORWARD "NO ERROR" SIGNAL TO DOWNSTREAM LOGIC
146
FORWARD "ERROR" SIGNAL TO DOWNSTREAM LOGIC
148

FIG. 5

150

CHECK BIT	PARITY	DATA BITS OF THE DIGITAL WORD							
		0	1	2	3	4	5	6	7
$(C)ECC_0$	EVEN (XOR)	X	A	A	X	X	A	X	X
$(C)ECC_1$	EVEN (XOR)	X	X	A	X	A	X	X	A
$(C)ECC_2$	EVEN (XOR)	A	X	X	A	X	A	X	A
$(C)ECC_3$	EVEN (XOR)	A	A	X	X	A	X	A	X

FIG. 6